AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 2, line 10 as follows:

The clock and data recovery circuit 10 may comprise a phase lock loop or delay lock loop that aligns the edges of the extracted clock, for example the rising edge, with the transition edge of the incoming data. In this instance the falling edge of the clock is approximately in the middle of the incoming data symbol. In this instance the retimer 20 may comprise, by way of example, a falling edge ~~flip flop~~ flip-flop that is triggered to recover the transmitted data on the falling edge of the clock.

Please amend the paragraph beginning on page 2, line 30 as follows:

For example, FIG. 2 is a simplified block diagram of a conventional one tap decision feedback equalizer 200 where a summer 210 combines the incoming data 220 with a feedback signal 230. A slicer 240 converts the output of the summer (soft decision) to a binary signal. A ~~flip flop~~ flip-flop 250 recovers the data from the binary signal in response to a clock 260. A multiplier 270 scales the recovered data by an equalization coefficient (g1) to generate the feedback signal 230 (typically a negative number) that is then combined with incoming data. The equalizer therefore serves to subtract a previous symbol from a current symbol to reduce or eliminate channel induced distortion such as inter-symbol interference.

Please amend the paragraph beginning on page 3, line 9 as follows:

In conventional receivers the extracted clock from the clock and data recovery circuit drives the ~~flip flop~~ flip-flop to recover equalized data. For example, FIG. 3 is a simplified block diagram of a decision feedback equalizer and clock and data recovery circuit based receiver 300. In this receiver incoming data is again amplified by one or more buffer stages 310. The clock and data recovery circuit 320 generates an extracted clock 330 from the amplified data (D1) and drives the decision feedback equalizer ~~flip flop~~ flip-flop 340 that recovers the equalized (D2) data provided by slicer 350.

Please amend the paragraph beginning on page 3, line 19 as follows:

In the illustrated receiver the clock and data recovery circuit 320 aligns the rising edge of the extracted clock 330 with the transition edge of the amplified data D1. In practice, however, the rising edge of the extracted clock 330 should be aligned with the equalized data (D2) output by the slicer 350 for proper data recovery by ~~flip flop~~ flip-flop 340. Therefore, the time delay through summer 360 and slicer 350 should be equal to the time delay through buffer stage(s) 310 to ensure that the input data (D2) and clock signal 330 of ~~flip flop~~ flip-flop 340 are aligned to properly recover the equalizer data.

Please amend the paragraph beginning on page 5, line 34 as follows:

In this embodiment, the binary signal output by the slicer 460 directly drives the data input of ~~flip flop~~ flip-flop 470 as well as the clock and data recovery circuit 420. The clock and data recovery circuit 420 therefore generates an extracted clock signal from the binary signal (D3) output by the slicer rather than from the incoming data 440 as is done in conventional receivers (see FIG. 3). The extracted clock output by the clock and data recovery circuit 420 is then used to clock the decision feedback equalizer ~~flip flop~~ flip-flop 470 that recovers the data from the binary signal (D3) in response to the extracted clock.

Please amend the paragraph beginning on page 6, line 11 as follows:

The clock and data recovery circuit 420 may automatically align the rising edge of the extracted clock, for example, with transitions in the binary signal (D3) output by the slicer 460. Therefore, the illustrated embodiment may maintain the proper timing relationship between the ~~flip flop~~ flip-flop 470 drive data (D3) and clock (i.e. the extracted clock) to ensure proper data recovery without the need for additional delay matching stages. The elimination of high speed delay matching circuits reduces the power consumption and dic area of the receiver.

Please amend the paragraph beginning on page 6, line 21 as follows:

In the illustrated embodiment a multiplier 480 scales the recovered equalized data output by the ~~flip flop~~ flip-flop 470 by an equalization coefficient (g1) to generate the equalized feedback signal 450. The value of the equalization coefficient depends on the level of inter-symbol

interference that is present in the incoming data. Typically the absolute value of the equalization coefficient (usually a negative number) increases with increasing inter-symbol interference. In one embodiment a real time optimization loop (not shown), such as a least mean square optimization loop, monitors the bit error rate of the incoming signal and adjusts the value of the equalization coefficient in response to changes in the bit error rate.

Please amend the paragraph beginning on page 11, line 13 as follows:

As the frequency of the output signal 515(b) of the voltage control oscillator 515 increases, its edges come sooner in time (i.e., the edges advance in time). Thus, for example, the rising edges of the output signal 515(b) of the voltage control oscillator 515 come in better alignment with the transitions or other reference points in the data signal 565. The feedback may, therefore, insure that the data signal and the output signal 515(b) of the voltage control oscillator 515 have the desired phase relationship for retiming the data via a data retimer (e.g. ~~flip-flop~~ flip-flop 470 of FIG. 4). When the desired phase relationship is reached via the feedback, then the loop may be deemed to be locked.